Section 16. Quadrature Encoder Interface (QEI)

HIGHLIGHTS

This section of the manual contains the following major topics:

16.1 Module Introduction

16.1.1 Features Overview

Quadrature encoders (a.k.a. Incremental encoders or Optical encoders) are used in position and speed detection of rotating motion systems. Quadrature encoders enable closed loop control of many motor control applications, such as Switched Reluctance (SR) motor and AC Induction Motor (ACIM).

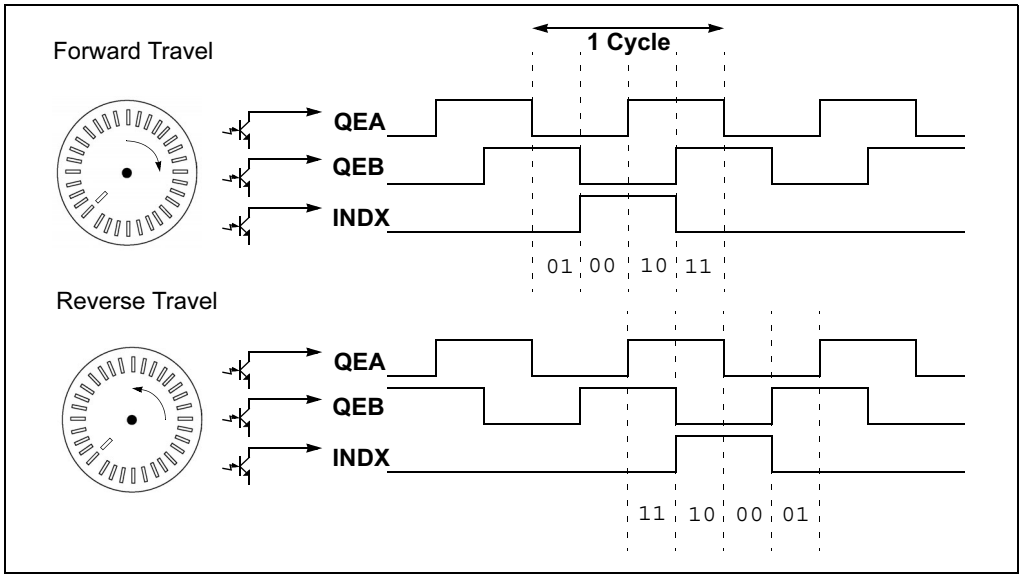
A typical incremental encoder includes a slotted wheel attached to the shaft of the motor and an emitter/detector module sensing the slots in the wheel. Typically, three outputs, termed: Phase A, Phase B and INDEX, provide information that can be decoded to provide information on the movement of the motor shaft including distance and direction.

The two channels, Phase A (QEA) and Phase B (QEB), have a unique relationship. If Phase A leads Phase B, then the direction (of the motor) is deemed positive or forward. If Phase A lags Phase B then the direction (of the motor) is deemed negative or reverse. A third channel, termed index pulse, occurs once per revolution and is used as a reference to establish an absolute position. See Figure 16-1 for a relative timing diagram of these three signals.

The quadrature signals produced by the encoder can have four unique states. These states are indicated for one count cycle in Figure 16-1. Note that the order of the states are reversed when the direction of travel is changed.

A Quadrature Decoder captures the phase signals and index pulse and converts the information into a numeric count of the position pulses. Generally, the count will increment when the shaft is rotating one direction and decrement when the shaft is rotating in the other direction.

Figure 16-1: Quadrature Encoder Interface Signals

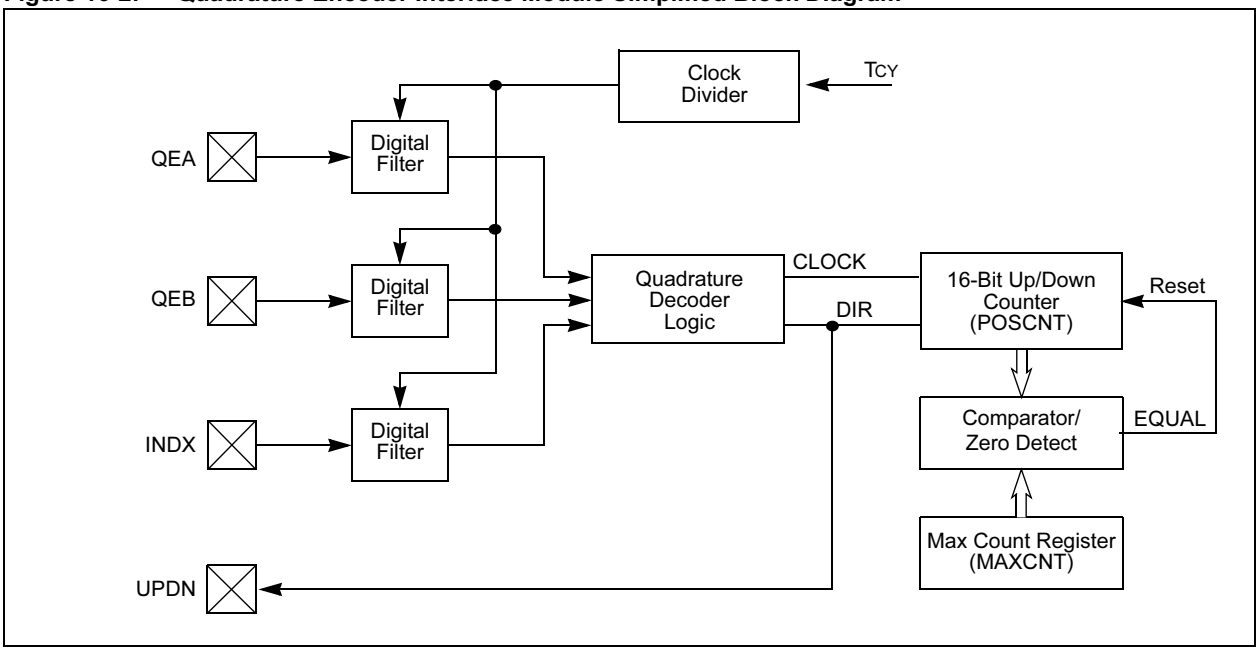


The Quadrature Encoder Interface (QEI) module provides an interface to incremental encoders. The QEI consists of quadrature decoder logic to interpret the Phase A and Phase B signals and an up/down counter to accumulate the count. Digital glitch filters on the inputs condition the input signal. Figure 16-2 depicts a simplified block diagram of the QEI Module.

The QEI module includes:

- Three input pins for two phase signals and index pulse
- Programmable digital noise filters on inputs
- Quadrature decoder providing counter pulses and count direction
- 16-bit up/down position counter
- Count direction status
- X2 and X4 count resolution
- 2 modes of position counter reset
- General Purpose16-bit timer/counter mode
- Interrupts generated by QEI or counter events

Figure 16-2: Quadrature Encoder Interface Module Simplified Block Diagram



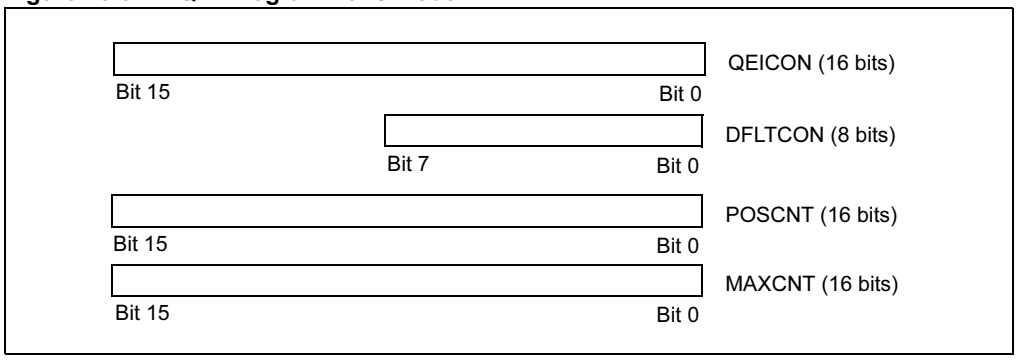
16.2 Control and Status Registers

The QEI module has four user-accessible registers. The registers are accessible in either byte or word mode. The registers are shown in Figure 16-3 and listed below:

- Control/Status Register (QEICON) – This register allows control of the QEI operation and status flags indicating the module state.
- Digital Filter Control Register (DFLTCON) – This register allows control of the digital input filter operation.
- Position Count Register (POSCNT) – This location allows reading and writing of the 16-bit position counter.
- Maximum Count Register (MAXCNT) – The MAXCNT register holds a value that will be compared to the POSCNT counter in some operations.

Note:	The POSCNT register allows byte accesses, however, reading the register in byte mode may result in partially updated values in subsequent reads. Either use word mode reads/writes or ensure that the counter is not counting during byte operations.

Figure 16-3: QEI Programmer's Model



Register 16-1 and Register 16-3 define the QEI module control and digital filter control registers, QEICON and DFLTCON.

Register 16-1: QEICON: QEI Control Register

Upper Byte:							
R/W-0	U-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
CNTERR	—	QEISIDL	INDEX	UPDN	QEIM<2:0>		
bit 15							bit 8

Lower Byte:							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SWPAB	PCDOUT	TQGATE	TQCKPS<1:0>		POSRES	TQCS	UDSRC
bit 7							bit 0

bit 15 **CNTERR:** Count Error Status Flag bit
1 = Position count error has occurred
0 = No position count error has occurred
(CNTERR flag only applies when QEIM<2:0> = '110' or '100')

bit 14 **Unimplemented:** Read as '0'

bit 13 **QEISIDL:** Stop in Idle Mode bit
1 = Discontinue module operation when device enters Idle mode
0 = Continue module operation in Idle mode

bit 12 **INDEX:** Index Pin State Status bit (Read Only)
1 = Index pin is High
0 = Index pin is Low

bit 11 **UPDN:** Position Counter Direction Status bit
1 = Position Counter Direction is positive (+)
0 = Position Counter Direction is negative (-)
(Read only bit when QEIM<2:0> = '1XX')
(Read/Write bit when QEIM<2:0> = '001')

bit 10-8 **QEIM<2:0>:** Quadrature Encoder Interface Mode Select bits
111 = Quadrature Encoder Interface enabled (x4 mode) with position counter reset by match (MAXCNT)
110 = Quadrature Encoder Interface enabled (x4 mode) with Index Pulse reset of position counter
101 = Quadrature Encoder Interface enabled (x2 mode) with position counter reset by match (MAXCNT)
100 = Quadrature Encoder Interface enabled (x2 mode) with Index Pulse reset of position counter
011 = Unused (Module disabled)
010 = Unused (Module disabled)
001 = Starts 16-bit Timer
000 = Quadrature Encoder Interface/Timer off

bit 7 **SWPAB:** Phase A and Phase B Input Swap Select bit
1 = Phase A and Phase B inputs swapped
0 = Phase A and Phase B inputs not swapped

bit 6 **PCDOUT:** Position Counter Direction State Output Enable bit
1 = Position Counter Direction Status Output Enable (QEI logic controls state of I/O pin)
0 = Position Counter Direction Status Output Disabled (Normal I/O pin operation)

bit 5 **TQGATE:** Timer Gated Time Accumulation Enable bit
1 = Timer gated time accumulation enabled
0 = Timer gated time accumulation disabled

bit 4-3 **TQCKPS<1:0>:** Timer Input Clock Prescale Select bits
11 = 1:256 prescale value
10 = 1:64 prescale value
01 = 1:8 prescale value
00 = 1:1 prescale value
(Prescaler utilized for 16-bit timer mode only)

Register 16-1: QEICON: QEI Control Register (Continued)

bit 2 **POSRES:** Position Counter Reset Enable bit
1 = Index Pulse resets Position Counter
0 = Index Pulse does not reset Position Counter
(Bit only applies when QEIM<2:0> = 100 or 110)

bit 1 **TQCS:** Timer Clock Source Select bit
1 = External clock from pin QEA (on the rising edge)
0 = Internal clock (TCY)

bit 0 **UDSRC:** Position Counter Direction Selection Control bit
1 = QEB pin State Defines Position Counter Direction
0 = Control/Status bit, UPDN (QEICON<11>), Defines Timer Counter (POSCNT) direction
Note: When configured for QEI mode, control bit is a 'don't care'

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

Register 16-2: DFLTCON: Digital Filter Control Register (dsPIC30F6010 Only)

Upper Byte:							
U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	CEID
bit 15							bit 8

Lower Byte:							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QEOUT	QECK<2:0>			INDOUT	INDCK<2:0>		
bit 7							bit 0

bit 15-9 **Unimplemented:** Read as '0'

bit 8 **CEID:** Count Error Interrupt Disable bit
1 = Interrupts due to position count errors disabled
0 = Interrupts due to position count errors enabled

bit 7 **QEOUT:** QEA/QEB Digital Filter Output Enable bit
1 = Digital filter outputs enabled
0 = Digital filter outputs disabled (Normal pin operation)

bit 6-4 **QECK<2:0>:** QEA/QEB Digital Filter Clock Divide Select bits
111 = 1:256 Clock Divide
110 = 1:128 Clock Divide
101 = 1:64 Clock Divide
100 = 1:32 Clock Divide
011 = 1:16 Clock Divide
010 = 1:4 Clock Divide
001 = 1:2 Clock Divide
000 = 1:1 Clock Divide

bit 3 **INDOUT:** Index Channel Digital Filter Output Enable bit
1 = Digital filter output is enabled
0 = Digital filter output is disabled (Normal pin operation)

bit 2-0 **INDCK<2:0>:** Index Channel Digital Filter Clock Divide Select bits
111 = 1:256 Clock Divide
110 = 1:128 Clock Divide
101 = 1:64 Clock Divide
100 = 1:32 Clock Divide
011 = 1:16 Clock Divide
010 = 1:4 Clock Divide
001 = 1:2 Clock Divide
000 = 1:1 Clock Divide

Note: The available control bits in the DFLTCON Register may vary depending on the dsPIC30F device that is used. Refer to Register 16-2 and Register 16-3 for details.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

Register 16-3: DFLTCON: Digital Filter Control Register (All dsPIC30F devices except dsPIC30F6010)

Upper Half:							
U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	IMV<1:0>		CEID
bit 15							bit 8

Lower Half:					
R/W-0	R/W-0	U-0	U-0	U-0	U-0
QEOUT	QECK<2:0>	—	—	—	—
bit 7					bit 0

bit 15-11 **Unimplemented:** Read as '0'

bit 10-9 **IMV<1:0>:** Index Match Value – These bits allow the user to specify the state of the QEA and QEB input pins during an Index pulse when the POSCNT register is to be reset.
In 4X Quadrature Count Mode:
IMV1= Required State of Phase B input signal for match on index pulse
IMV0= Required State of Phase A input signal for match on index pulse
In 2X Quadrature Count Mode:
IMV1= Selects Phase input signal for Index state match (0 = Phase A, 1 = Phase B)
IMV0= Required State of the selected Phase input signal for match on index pulse

bit 8 **CEID:** Count Error Interrupt Disable
1 = Interrupts due to count errors are disabled
0 = Interrupts due to count errors are enabled

bit 7 **QEOUT:** QEA/QEB/INDX pin Digital Filter Output Enable
1 = Digital filter outputs enabled
0 = Digital filter outputs disabled (normal pin operation)

bit 6-4 **QECK<2:0>:** QEA/QEB/INDX Digital Filter Clock Divide Select Bits
111 = 1:256 Clock Divide
110 = 1:128 Clock Divide
101 = 1:64 Clock Divide
100 = 1:32 Clock Divide
011 = 1:16 Clock Divide
010 = 1:4 Clock Divide
001 = 1:2 Clock Divide
000 = 1:1 Clock Divide

bit 3-0 **Unimplemented:** Read as '0'

Note: The available control bits in the DFLTCON Register may vary depending on the dsPIC30F device that is used. Refer to Register 16-2 and Register 16-3 for details.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
y = Value set from configuration bits on POR or BOR			

16.3 Programmable Digital Noise Filters

The digital noise filter section is responsible for rejecting noise on the incoming index and quadrature signals. Schmitt trigger inputs and a three-clock cycle delay filter combine to reject low level noise and large, short duration noise spikes that typically occur in noise-prone applications such as a motor system applications.

The filter ensures that the filtered output signals are not permitted to change until a stable value has been registered for three consecutive filter cycles.

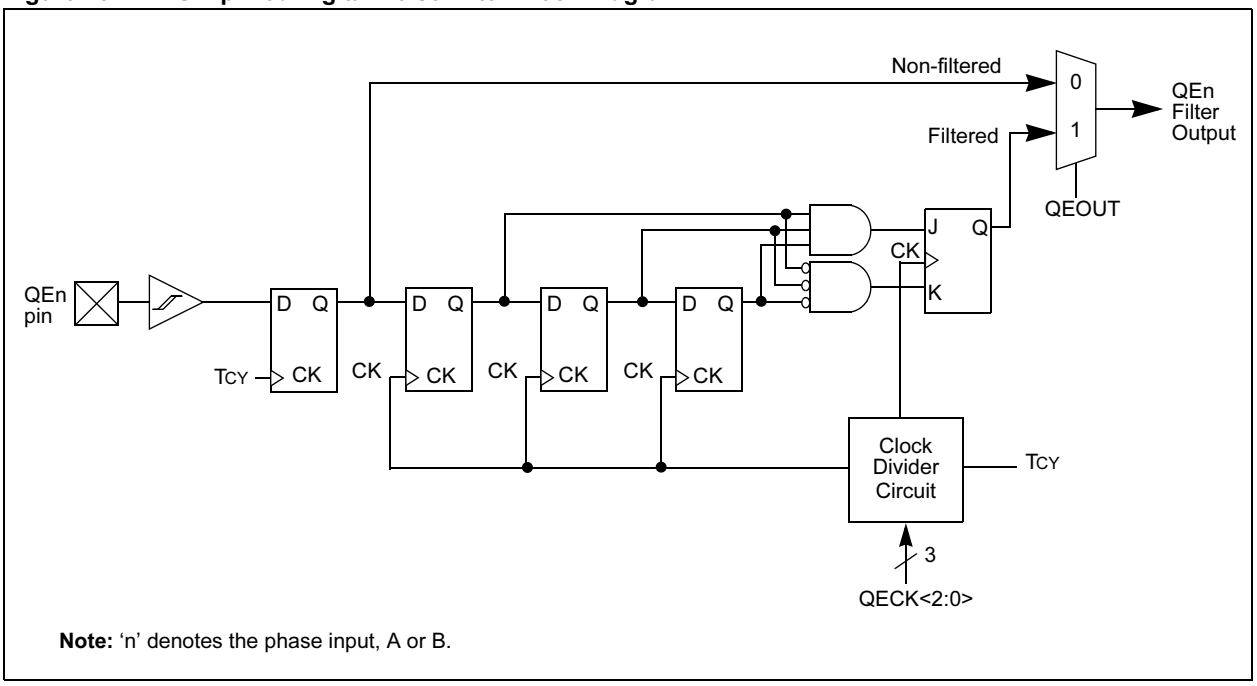
The rate of the filter clocks determines the low passband of the filter. A slower filter clock results in a passband rejecting lower frequencies than a faster filter clock. The filter clock is the device FCY clock divided by a programmable divisor.

Setting the QEOUT bit (DFLTCON<7>) enables the filter for channels QEA and QEB. The QECK<2:0> bits (DFLTCON<6:4>) specify the filter clock divisor used for channels QEA and QEB. Setting the INDOUT bit (DFLTCON<3>) enables the filter for the index channel. The INDCK<2:0> bits (DFLTCON<2:0>) specify the filter clock divisor used for the index channel. At reset, the filters for all channels are disabled.

Some devices do not have separate control bits for the QEx input digital filters and the INDX input digital filter. For these devices, the QEOUT and QECK<2:0> control bits set the digital filter characteristics for both the QEA/QEB and INDX pins. See Register 16-2 and Register 16-3 for more information.

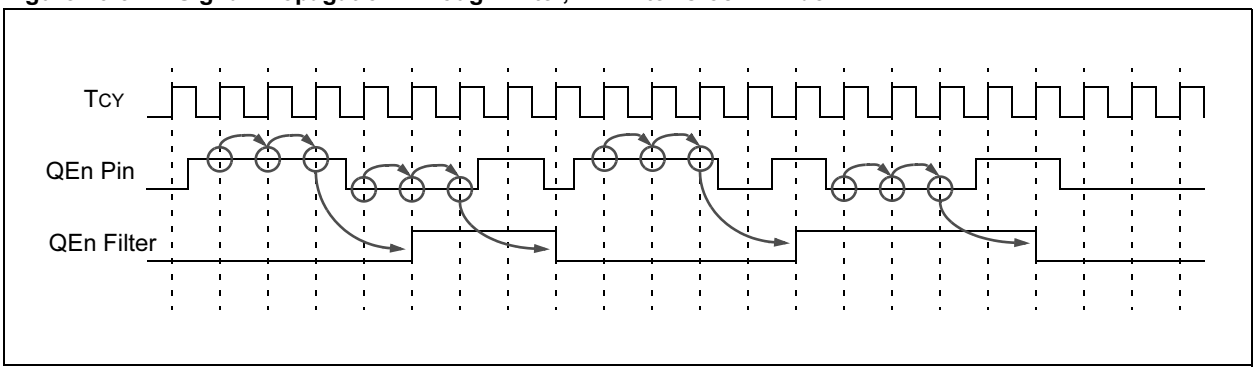
Figure 16-4 depicts a simplified block diagram for the digital noise filter.

Figure 16-4: Simplified Digital Noise Filter Block Diagram



Note: 'n' denotes the phase input, A or B.

Figure 16-5: Signal Propagation Through Filter, 1:1 Filter Clock Divide



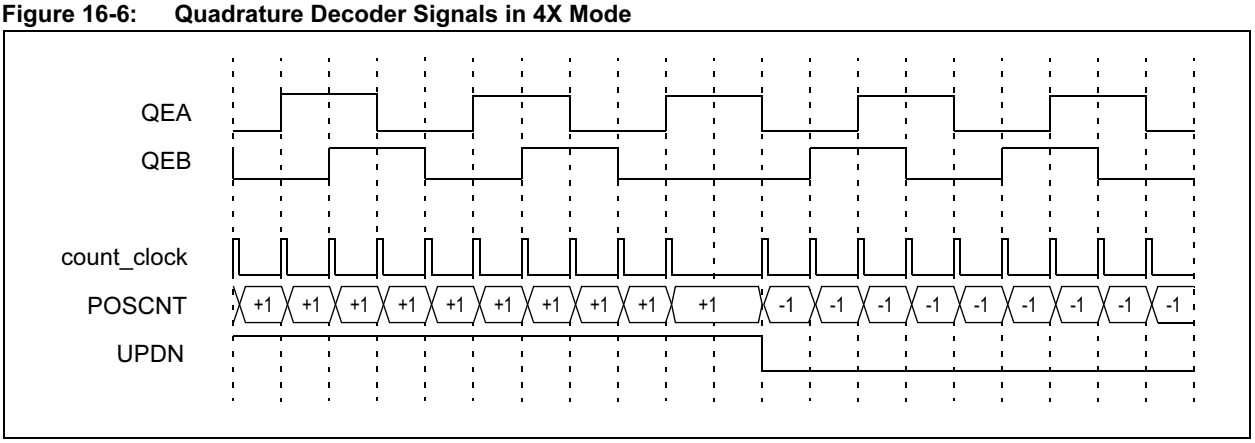
16.4 Quadrature Decoder

Position measurement modes are selected when QEIM2 = 1 (QEICON<10>).

When QEIM1 = 1 (QEICON<9>), the 'x4' measurement mode is selected and the QEI logic clocks the position counter on both edges of the Phase A and Phase B input signals.

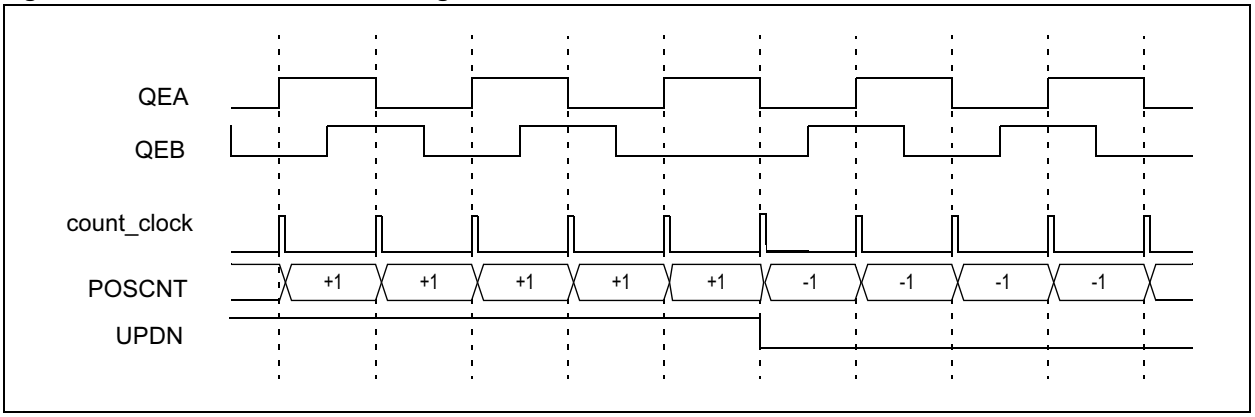
The 'x4' measurement mode provides for finer resolution data (more position counts) to determine the encoder position.

Figure 16-6: Quadrature Decoder Signals in 4X Mode



When QEIM1 = 0, the 'x2' measurement mode is selected and the QEI logic only looks at the rising and falling edge of the Phase A input for the position counter increment rate. Every rising and falling edge of the Phase A signal causes the position counter to increment or decrement. The Phase B signal is still utilized for the determination of the counter direction, exactly like the x4 measurement mode.

Figure 16-7: Quadrature Decoder Signals in 2X Mode



16.4.1 Explanation of Lead/Lag Test

The lead/lag test is performed by the quadrature decoder logic to determine the phase relationship of the QEA and QEB signals and hence whether to increment or decrement the POSCNT register. The Table 16-1 clarifies the lead/lag test.

Table 16-1: Lead/Lag Test Description

Present Transition	Previous Transition	Condition	Action	
QEA↑	QEB↓	QEA leads QEB channel	Set UPDN	Increment POSCNT
	QEB↑	QEA lags QEB channel	Clear UPDN	Decrement POSCNT
	QEA↓	Direction Change	Toggle UPDN	Increment or Decrement POSCNT
QEA↓	QEB↓	QEA lags QEB channel	Clear UPDN	Decrement POSCNT
	QEB↑	QEA leads QEB channel	Set UPDN	Increment POSCNT
	QEA↑	Direction Change	Toggle UPDN	Increment or Decrement POSCNT
QEB↑	QEA↓	QEA lags QEB channel	Clear UPDN	Decrement POSCNT
	QEA↑	QEA leads QEB channel	Set UPDN	Increment POSCNT
	QEB↓	Direction Change	Toggle UPDN	Increment or Decrement POSCNT
QEB↓	QEA↓	QEA leads QEB channel	Set UPDN	Increment POSCNT
	QEA↑	QEA lags QEB channel	Clear UPDN	Decrement POSCNT
	QEB↑	Direction Change	Toggle UPDN	Increment or Decrement POSCNT

16.4.2 Count Direction Status

As mentioned in the previous section, the QEI logic generates an UPDN signal based upon the Phase A and Phase B time relationship. The UPDN signal may be output on an I/O pin.

Setting the PCDOUT bit (QEICON<6>) and clearing the appropriate TRIS bit associated with the pin will cause the UPDN signal to drive the output pin.

In addition to the output pin, the state of this internal UPDN signal is supplied to a SFR bit QEICON<11> as a Read-Only bit, notated as UPDN.

16.4.3 Encoder Count Direction

The direction of quadrature counting is determined by the SWPAB bit (QEICON<7>). If the SWPAB = 0, the Phase A input is fed to the A input of the quadrature counter and the Phase B input is fed to the B input of the quadrature counter. Therefore as the Phase A signal leads the Phase B signal, the quadrature counter is incremented on each edge. This (A signal leads the B signal) is defined as the forward direction of motion. Setting the SWPAB bit, (QEICON<7>), to a logic 1 causes the Phase A input to be fed to the B input of the quadrature counter and the Phase B signal to be fed to the A input of the quadrature counter. Therefore, if the Phase A signal leads the Phase B signal at the dsPIC30F device pins, the Phase A input to the quadrature counter will now lag the Phase B input. This is recognized as rotation in the reverse direction and the counter will be decremented on each quadrature pulse.

16.4.4 Quadrature Rate

The RPM of the position control system will vary. The RPMs along with the quadrature encoder line count determine the frequency of the QEA and QEB input signals. The quadrature encoder signals can be decoded such that a count pulse is generated for every quadrature signal edge. This allows an angular position measurement resolution of up to 4 times the encoder line count. For example: a 6,000 RPM motor utilizing a 4096 line encoder yields a quadrature count rate of: ((6000/60) * (4096*4)) = 1.6384 MHz. Likewise, a 10,000 RPM motor utilizing a 8,192 line encoder yields a quadrature count rate of: ((10000/60) * (8192*4)) = 5.46 MHz.

The QEI allows a quadrature frequency of up to FCY/3. For example, if FCY = 30 MHz, the QEA and QEB signals may have a maximum frequency of 10 MHz. Refer to the "Electrical Specifications" section of the device data sheet for further details.

16.5 16-bit Up/Down Position Counter

The 16-bit Up/Down Counter counts up or down on every count pulse which is generated by the quadrature decoder logic. The counter then acts as an integrator, whose count value is proportional to position. The direction of the count is determined by the quadrature decoder.

The user software may examine the contents of the count by reading the POSCNT register. The user software may also write to the POSCNT register to initialize a count.

Changing the QEIM bits does not affect the position counter register contents.

16.5.1 Using the Position Counter

The system may utilize position counter data in one of several methods. In some systems, the position count is accumulated consistently and taken as an absolute value representing the total position of the system. For a typical example, assume that a quadrature encoder is affixed to a motor controlling the print head in a printer. In operation, the system is initialized by moving the print head to the maximum left position and resetting the POSCNT register. As the print head moves to the right, the quadrature encoder will begin to accumulate counts in the POSCNT register. As the print head moves to the left, the accumulated count will decrease. As the print head reaches the right most position, the maximum position count should be reached. If the maximum count is less than 2^{16}, the QEI module can encode the entire range of motion.

If, however, the maximum count is more than 2^{16}, the additional count precision must be captured by the user software. Generally, to accomplish this, the module is set into a mode where it resets the counter at match of a maximum count. QEIM0 = `1` enables modes where the MAXCNT register is used to reset the position counter. When the counter reaches a pre-determined maximum count while incrementing or reaches zero while decrementing, the count is reset and an interrupt is generated to allow the user software to increment or decrement a software counter containing the most significant bits of the position count. The maximum count can be `0xFFFF`, to enable a full range of the QEI counter and software counter or some smaller value of significance, such as the number of counts for one encoder revolution.

In other systems, the position count may be cyclic. The position count is only used to reference the position of the wheel within number of rotations determined by the index pulse. For example, a tool platform moved by a screw rod uses a quadrature encoder attached to the screw rod. In operation, the screw may require 5.5 rotations to achieve the desired position. The user software will detect 5 index pulses to count the full rotations and use the position count to measure the remaining half rotation. In this method, the index pulse resets the position counter to initialize the counter at each rotation and generates an interrupt for each rotation. QEIM0 = `0` enables these modes.

16.5.2 Using MAXCNT to Reset the Position Counter

When the QEIM0 bit is '1', the position counter will reset on a match of the position count with predetermined high and low values. The index pulse reset mechanism is not utilized.

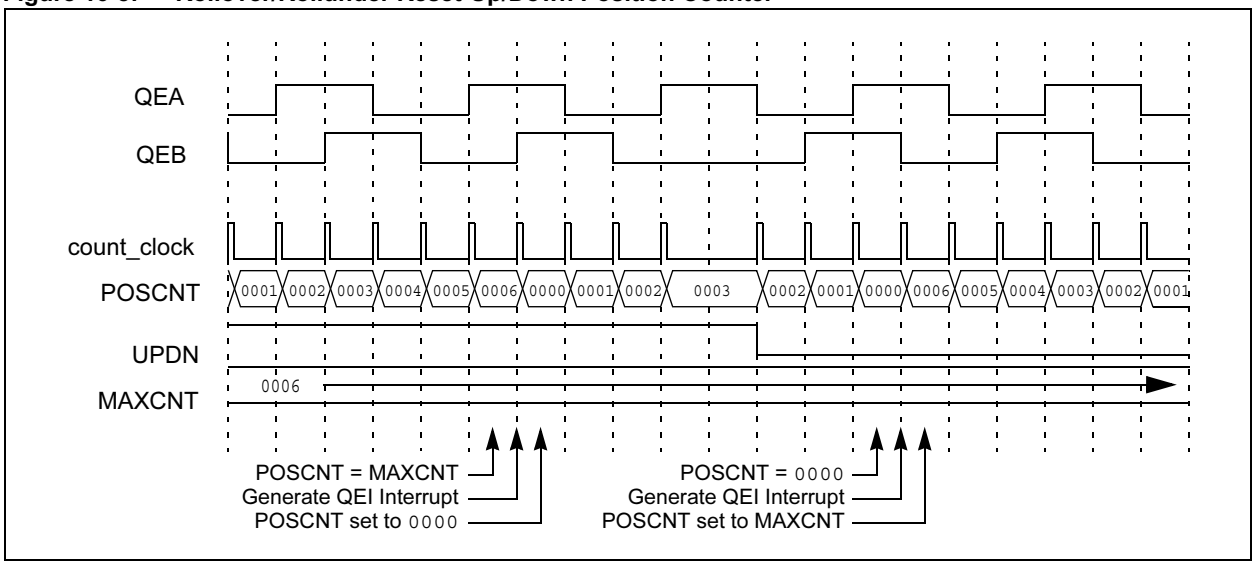
For this mode the position counter reset mechanism operates as follows: (See Figure 16-8 for related timing details).

- If the encoder is traveling in the forward direction e.g., QEA leads QEB, and the value in the POSCNT register matches the value in the MAXCNT register, POSCNT will reset to zero **on the next occurring quadrature pulse edge that increments POSCNT. An interrupt event is generated on this rollover event.**
- If the encoder is travelling in the reverse direction e.g., QEB leads QEA, and the value in the POSCNT register counts down to '0', the POSCNT is loaded with the value in the MAXCNT register **on the next occurring quadrature pulse edge that decrements POSCNT. An interrupt event is generated on this underflow event.**

When using MAXCNT as a position limit, remember the position counter will count at either 2X or 4X of the encoder counts. For standard rotary encoders, the appropriate value to write to MAXCNT would be 4N – 1 for 4x position mode and 2N – 1 for 2x position mode, where N is the number of counts per revolution of the encoder.

For absolute position information where the range of the system exceeds 2^{16}, it is also appropriate to load a value of `0xFFFF` into the MAXCNT register. The module will generate an interrupt on rollover or underflow of the position counter.

Figure 16-8: Rollover/Rollunder Reset-Up/Down Position Counter

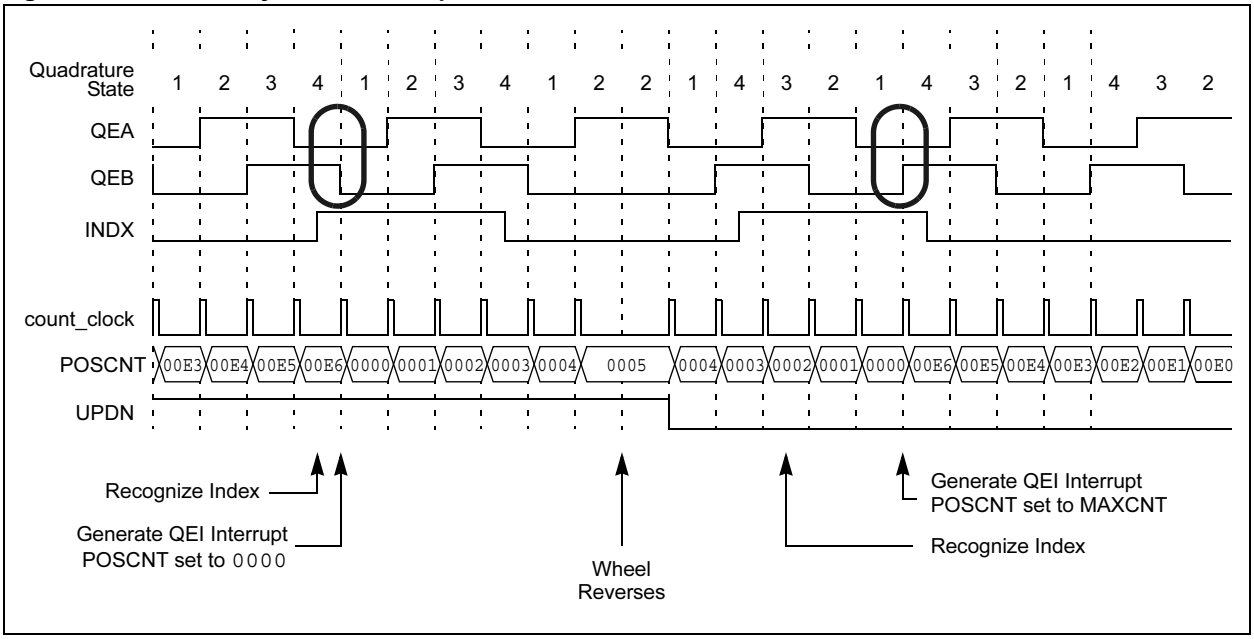


16.5.3 Using Index to Reset Position Counter

When QEIM<0> = 0, the index pulse is utilized for resetting the position counter. For this mode the position counter reset mechanism operates as follows: (See Figure 16-9 for related timing details).

- The position count is reset each time an index pulse is received on the INDEX pin.
- If the encoder is travelling in the forward direction e.g., QEA leads QEB, POSCNT is reset to '0'.
- If the encoder is travelling in the reverse direction e.g., QEB leads QEA, the value in the MAXCNT register is loaded into POSCNT.

Figure 16-9: Reset by Index Mode-Up/Down Position Counter



16.5.3.1 Index Pulse Detection Criteria

Incremental encoders from different manufacturers use differing timing for the index pulse. The index pulse may be aligned to any of the 4 quadrature states and may have a pulse width of either a full cycle (4 quadrature states), a half cycle (2 quadrature states) or a quarter cycle (1 quadrature state). Index pulses of a full cycle width or a half cycle width are normally termed 'ungated' and index pulses of a quarter cycle width are normally termed 'gated'.

Regardless of the type of index pulse provided, the QEI maintains symmetry of the count as the wheel reverses direction. This means the index pulse must reset the position counter at the same relative quadrature state transition as the wheel rotates in the forward or reverse direction.

For example, in Figure 16-9, the first index pulse is recognized and resets POSCNT as the quadrature state changes from 4 to 1 as highlighted in the diagram. The QEI latches the state of this transition. Any subsequent index pulse detection will use that state transition for the reset.

As the wheel reverses, the index pulse again occurs, however the reset of the position counter cannot occur until the quadrature state changes from 1 to 4, again highlighted in the diagram.

Note:	The QEI index logic ensures that the POSCNT register is always adjusted at the same position relative to the index pulse, regardless of the direction of travel.

16.5.3.2 IMV Control Bits

The IMV<2:0> control bits are available on some dsPIC devices that have the QEI module. (See Register 16-3). These control bits allow the user to select the state of the QEA and QEB signals for which an index pulse reset will occur.

Devices that do not have these control bits will select the QEA and QEB states automatically during the first occurrence of an index pulse.

16.5.3.3 Index Pulse Status

The INDEX bit (QEICON<12>) provides status of the logic state on the index pin. This status bit is very useful in position control systems during the “homing” sequence, where the system searches for a reference position. The index bit indicates the status of the index pin after being processed by the digital filter, if it is enabled.

16.5.3.4 Using the Index Pin and MAXCNT for Error Checking

When the counter operates in reset on index pulse mode, the QEI will also detect POSCNT register boundary conditions. This may be used to detect system errors in the incremental encoder system.

For example, assume a wheel encoder has 100 lines. When utilized in x4 measurement mode and reset on the index pulse, the counter should count from 0 to 399 (`0x018E`) and reset. If the POSCNT register ever achieves the values of `0xFFFF` or `0x0190`, some sort of system error has occurred.

The contents of the POSCNT register is compared with MAXCNT + 1, if counting up, and with `0xFFFF`, if counting down. If the QEI detects one of these values, a position count error condition is generated by setting the CNTERR bit (QEICON<15>) and optionally generating a QEI interrupt.

If the CEID control bit (DFLTCON<8>) is cleared (default), then a QEI interrupt will be generated when a position count error is detected. If the CEID control bit is set, then an interrupt will not occur.

The position counter continues to count encoder edges after detecting a position count error. No interrupt is generated for subsequent position count error events until CNTERR is cleared by the user.

16.5.3.5 Position Counter Reset Enable

The position counter reset enable bit, POSRES (QEICON<2>) enables reset of the position counter when the index pulse is detected. This bit only applies when the QEI module is configured for modes, QEIM<2:0> = ‘`100`’ or ‘`110`’.

If the POSRES bit is set to a logic ‘1’ then the position counter is reset when the index pulse is detected as described in this section.

If the POSRES bit is set to a logic ‘0’, then the position counter is not reset when the index pulse is detected. The position counter will continue counting up or down and be reset on the rollover or underflow condition. The QEI continues to generate interrupts on the detection of the index pulse.

16.6 Using QEI as an Alternate 16-bit Timer/Counter

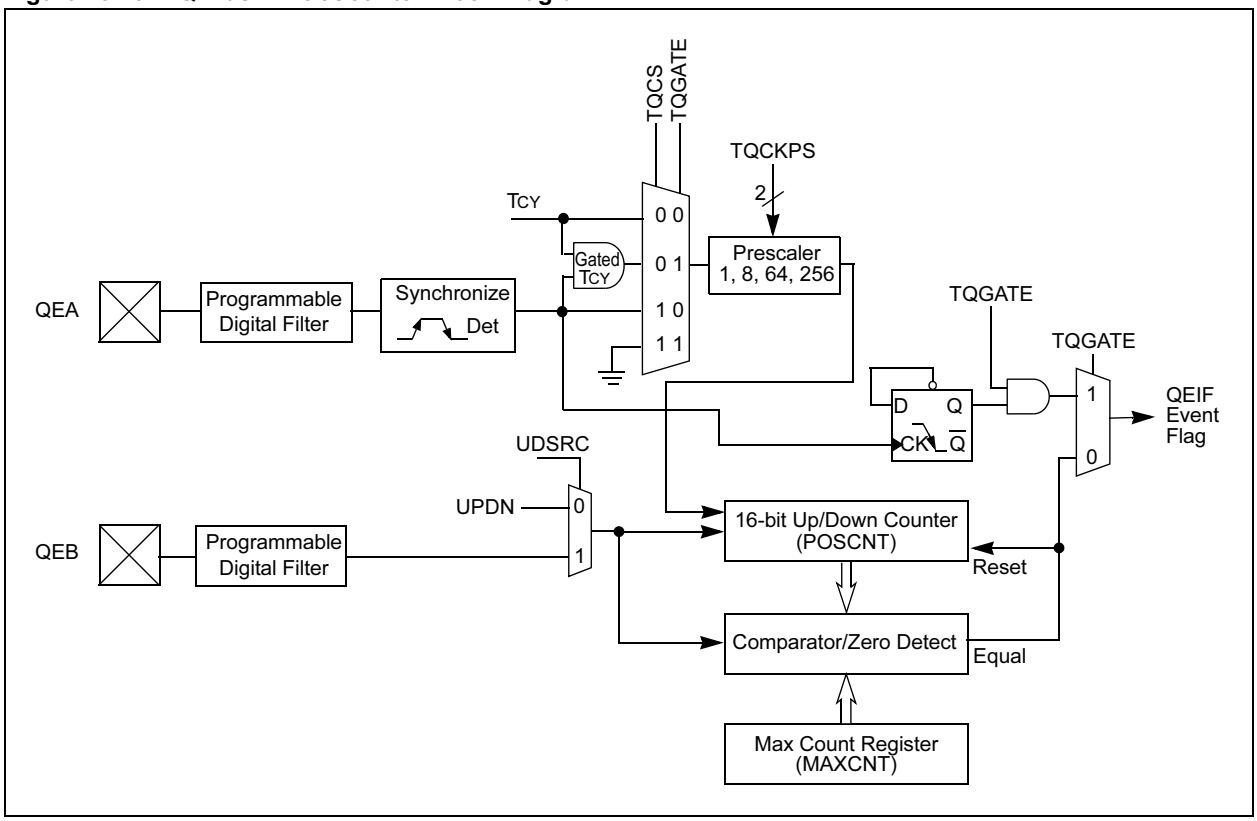
When the QEI module is configured QEIM<2:0> = 001, the QEI function is disabled and the QEI module is configured as a 16-bit timer/counter. The setup and control for the auxiliary timer is accomplished through the QEICON register.

The QEI timer functions similar to the other dsPIC30F timers. Refer to **Section 12. "Timers"** for a general discussion of timers.

When configured as a timer, the POSCNT register serves as a timer register similar to the TMRn registers of the GP timers. The MAXCNT register serves as a period register similar to the PRn registers of the GP timers. When a timer/period register match occurs, the QEIF flag asserts.

Note:	Changing operational modes, i.e., from QEI to Timer or Timer to QEI will not affect the Timer/Position Count Register contents.

Figure 16-10: QEI as Timer/Counter Block Diagram



16.6.1 Up/Down Timer Operation

The QEI timer can increment or decrement. This is a unique feature over most other timers.

When the timer is configured to count up, the timer (POSCNT) will increment until the count matches the period register (MAXCNT). The timer resets to zero and restarts incrementing.

When the timer is configured to count down, the timer (POSCNT) will decrement until the count matches the period register (MAXCNT). The timer resets to zero and restarts decrementing.

When the timer is configured to count down some general operation guidelines must be followed for correct operation.

1. The MAXCNT register will serve as the period match register but because the counter is decrementing, the desired match value is 2 count. For example, to count `0x1000` clocks, the period register must be loaded with `0xF000`.
2. On a match condition, the timer resets to zero.

Either an I/O pin or a SFR control bit specify the count direction control.

Control bit UDSRC (QEICON<0>) determines what controls the timer count direction state.

When UDSRC = `1`, the timer count direction is controlled from the QEB pin. If the QEB pin is '1', the count direction will be incrementing. If the QEB pin is '0', the count direction will be decrementing.

When UDSRC = `0`, the timer count direction is controlled from the UPDN bit (QEICON<11>). When UPDN = `1`, the timer increments. When UPDN = `0`, the timer decrements.

16.6.2 Timer External Clock

The TQCS bit (QEICON<1>) selects internal or external clock. The QEI timer can use the QEA pin as an external clock input when TQCS is set. The QEI timer does not support the external asynchronous counter mode. If using an external clock source the clock will automatically be synchronized to the internal instruction cycle (T_{CY}).

16.6.3 Timer Gate Operation

The QEA pin functions as a timer gate when the TQGATE bit (QEICON<5>) is set and TQCS is cleared.

In the event TQCS and TQGATE are concurrently set, the timer does not increment and does not generate an interrupt.

16.7 Quadrature Encoder Interface Interrupts

Depending on the mode of the QEI, the QEI will generate interrupts for the following events:

- When operating in reset on match mode, QEIM<2:0> = '`111`' and '`101`', an interrupt occurs on position counter rollover/underflow.
- When operating in reset on index mode, QEIM<2:0> = '`110`' and '`100`', an interrupt occurs on detection of index pulse and optionally when CNTERR bit is set.
- When operating as a Timer/Counter, QEIM<2:0> = '`001`', an interrupt occurs on a period match event or a timer gate falling edge event when TQGATE = `1`.

When a QEI interrupt event occurs, the QEIIF bit (IFS2<8>) is asserted and an interrupt will be generated if enabled. The QEIIF bit must be cleared in software.

Enabling the QEI interrupt is accomplished via the respective enable bit, QEIIE (IEC2<8>).

16.8 I/O Pin Control

Enabling the QEI module causes the associated I/O pins to come under the control of the QEI and prevents lower priority I/O functions such as Ports from affecting the I/O pin.

Depending on the mode specified by QEIM<2:0> and other control bits, the I/O pins may assume differing functions, as shown in Table 16-2 and Table 16-3.

Table 16-2: Quadrature Encoder Module Pinout I/O Descriptions

Pin Name	Pin Type	Buffer Type	Description
QEA	I I I	ST ST ST	Quadrature Encoder Phase A Input, or Auxiliary Timer External Clock Input, or Auxiliary Timer External gate Input
QEB	I I	ST ST	Quadrature Encoder Phase B Input, or Auxiliary Timer Up/Down select input
INDX	I	ST	Quadrature Encoder Index Pulse Input
UPDN	O		Position Up/Down Counter Direction Status, QEI mode

Legend: I = Input, O = Output, ST = Schmitt Trigger

Table 16-3: Module I/O Mode Functions

QEIM<2:0>	PCDOUT	UDSRC	TQGATE	TQCS	QEA pin	QEB pin	INDX pin	UPDN pin
000,010,011 Module Off	N/A	N/A	N/A	N/A				
001 Timer Mode	N/A	0	0	0				
		1	0	0		Input (UPDN)		
		0	1	0	Input (TQGATE) Port not disabled			
		1	1	0	Input (TQGATE) Port not disabled	Input (UPDN)		
		0	N/A	1	Input (TQCKI) Port not disabled			
		1	N/A	1	Input (TQCKI) Port not disabled	Input (UPDN)		
101,111 QEI Reset by count	0	N/A	N/A	N/A	Input (QEA)	Input (QEB)		
	1	N/A	N/A	N/A	Input (QEA)	Input (QEB)		Output (UPDN)
100,110 QEI Reset by Index	0	N/A	N/A	N/A	Input (QEA)	Input (QEB)	Input (INDX)	
	1	N/A	N/A	N/A	Input (QEA)	Input (QEB)	Input (INDX)	Output (UPDN)

Note: Empty slot indicates pin not used by QEI in this configuration,pin controlled by I/O port logic.

16.9 QEI Operation During Power Saving Modes

16.9.1 When the Device Enters Sleep

When the device enters Sleep mode, the QEI will cease all operations. POSCNT will stop at the current value. The QEI will not respond to active signals on the QEA, QEB, INDX or UPDN pins.

The QEICON register will remain unchanged.

If the QEI is configured as a timer/counter, QEIM<2:0> = '001', and the clock is provided externally, TQCS = 1, the module will also cease operation during Sleep mode.

When the module wakes up, the quadrature decoder will accept the next transition on the QEA or QEB signals and compare that transition to the last transition before Sleep to determine the next action.

16.9.2 When the Device Enters Idle

The module will enter a power saving state in Idle mode depending on the QEISIDL bit (QEICON<13>).

If QEICSIDL = 1, then the module will enter the power saving mode, similar to actions while entering Sleep mode.

If QEICSIDL = 0, then the module will not enter a power saving mode. The module will continue to operate normally while the device is in Idle mode.

16.10 Effects of a Reset

Reset forces module registers to their initial reset state. See Register 16-1 for all initialization and reset conditions for QEI module related registers.

The quadrature decoder and the POSCNT counter are reset to an initial state.

Table 16-4: Special Function Registers Associated with QEI

Name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on ALL Reset
QEICON	CNTERR	Unused	QEISIDL	INDX	UPDN	QEIM2	QEIM1	QEIM0	SWPAB	PCDOUT	TQGATE	TQCKPS1	TQCKPS0	POSRES	TQCS	UDSRC	0000 0000 0000 0000
DFLTCON	—	—	—	—	—	—	—	—	QEOUT	QECK2	QECK1	QECK0	INDOUT	INDCK2	INDCK1	INDCK0	---- ---- ---- ----
POSCNT	Position Count Register																0000 0000 0000 0000
MAXCNT	Maximum Count Register																1111 1111 1111 1111
ADPCFG	PCFG15	PCFG14	PCFG13	PCFG12	PCFG11	PCFG10	PCFG9	PCFG8	PCFG7	PCFG6	PCFG5	PCFG4	PCFG3	PCFG2	PCFG1	PCFG0	0000 0000 0000 0000
INTCON1	NSTDIS	—	—	—	—	OVATE	OVBTE	COVTE	—	—	—	MATHERR	ADDRERR	STKERR	OSCFAIL	—	0000 0000 0000 0000
INTCON2	ALTIVT	—	—	—	—	—	—	—	—	—	—	INT4EP	INT3EP	INT2EP	INT1EP	INT0EP	0000 0000 0000 0000
IFS2	—	—	—	FLTBIF	FLTAIF	LVDIF	DCIIF	QEIIF	PWMIF	C2IF	INT4IF	INT3IF	OC8IF	OC7IF	OC6IF	OC5IF	0000 0000 0000 0000
IEC2	—	—	—	FLTBIE	FLTAIE	LVDIE	DCIIE	QEIIE	PWMIE	C2IE	INT4IE	INT3IE	OC8IE	OC7IE	OC6IE	OC5IE	0000 0000 0000 0000
IPC10	—	FLTAIP<2:0>			—	LVDIP<2:0>			—	DCIIP<2:0>			—	QEIIP<2:0>			0100 0100 0100 0100

Note: The available control bits in the DFLTCON Register may vary depending on the dsPIC30F device that is used. Refer to Register 16-2 and Register 16-3 for details.

Note: On many devices, the QEI pins are multiplexed with analog input pins. You will need to ensure that the QEI pins are configured as digital pins using the ADPCFG control register.

16.11 Design Tips

Question 1: ***I have initialized the QEI, but the POSCNT Register does not seem to change when quadrature signals are applied to the QEA/QEB pins.***

Answer: On many devices, the QEI pins are multiplexed with analog input pins. You will need to ensure that the QEI pins are configured as digital pins using the ADPCFG control register.

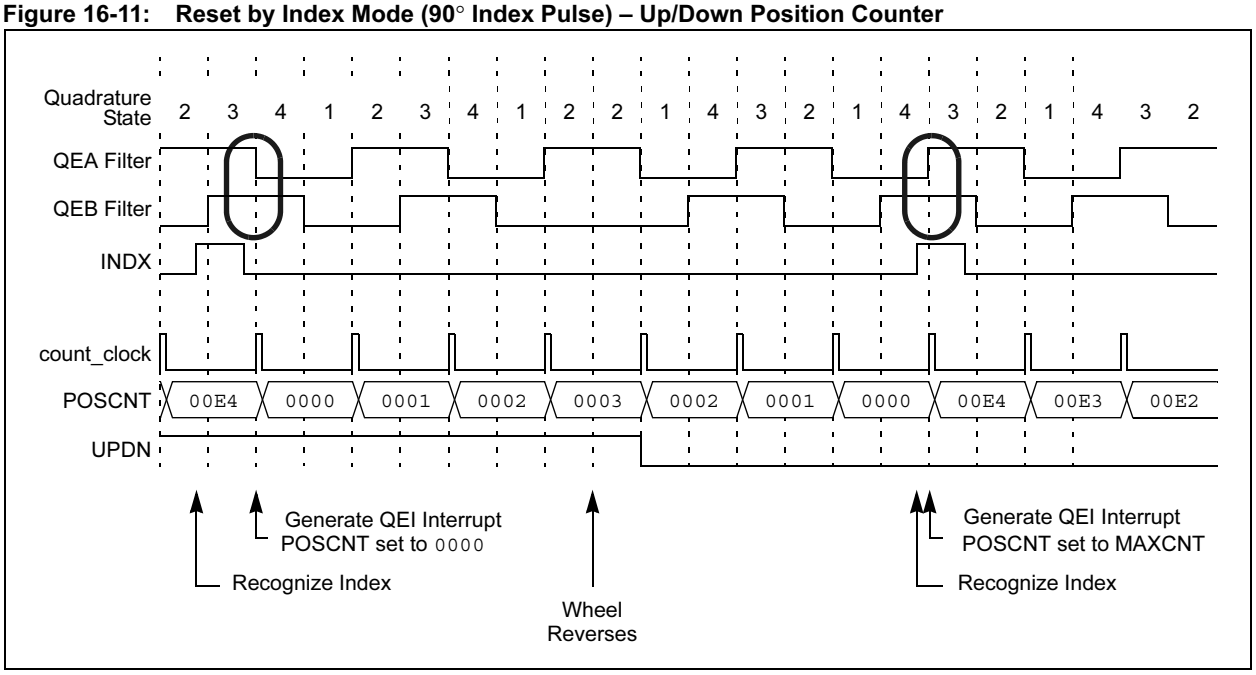
Question 2: ***How fast may my quadrature signals be?***

Answer: The answer depends on the setting of the filter parameters for the quadrature signals. QEI requires that quadrature signals frequency must be less than FCY/3 when no filter is used and Filter Frequency/6 when a filter is used.

Question: 3 ***My encoder has a 90° Index Pulse and the count does not reset properly.***

Answer: Depending on how the count clock is generated and which quadrature state transition is used for the index pulse, a 1/4 cycle index pulse may not be recognized before the required transition. To fix this, use a filter on the quadrature clocks which has a higher filter prescaler than that of the index pulse. This has the effect of delaying the quadrature clocks somewhat, allowing for proper detection of the index pulse.

Figure 16-11: Reset by Index Mode (90° Index Pulse) – Up/Down Position Counter



16.12 Related Application Notes

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the dsPIC30F Product Family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the Quadrature Encoder Interface (QEI) module are:

Title	Application Note #
Servo Control of a DC-Brush Motor	AN532
PIC18CXXX/PIC16CXXX DC Servomotor	AN696
Using the dsPIC30F for Vector Control of an ACIM	AN908

Note: Please visit the Microchip web site (www.microchip.com) for additional Application Notes and code examples for the dsPIC30F Family of devices.

16.13 Revision History

Revision A

This is the initial released revision of this document.

Revision B

This revision provides expanded information for the dsPIC30F Quadrature Encoder Interface (QEI) module.

Revision C

This revision incorporates all known errata at the time of this document update.

NOTES: